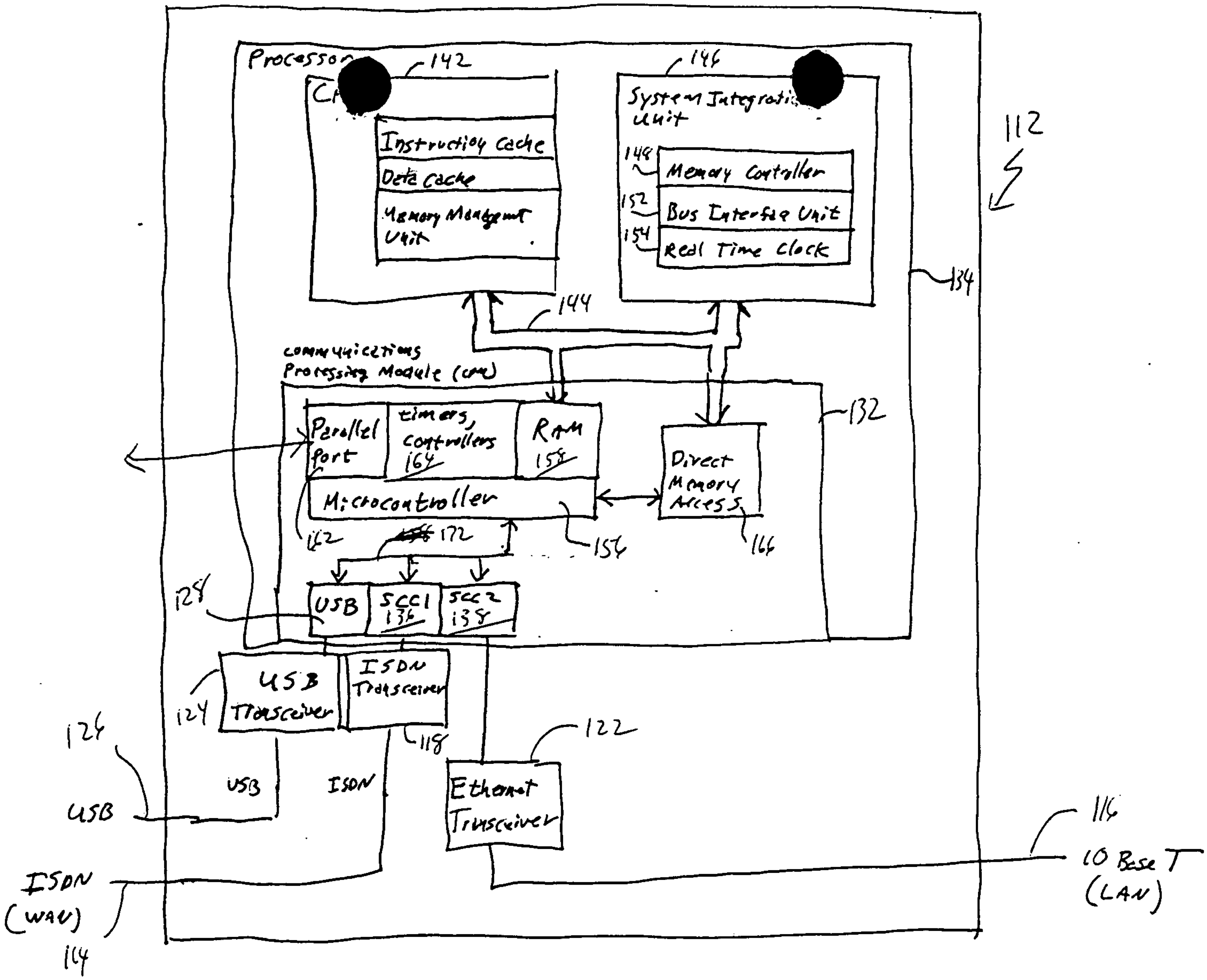


Processor
142
CP
Instruction cache
Data cache
Memory Management Unit
146
System Integrati
Unit
148
Memory Controller
152
Bus Interface Unit
154
Real Time Clock
112
134
144
Communications Processing Module (CPM)
132
Parallel Port
timers, controllers
164
RAM
158
Microcontroller
Direct Memory Access
162
172
156
166
128
USB
SCC1
136
SCC2
138
USB Transceiver
ISDN Transceiver
124
118
126
USB
ISDN
122
Ethernet Transceiver
116
10 Base T
(LAN)
ISDN
(WAN)
114

Fig 1

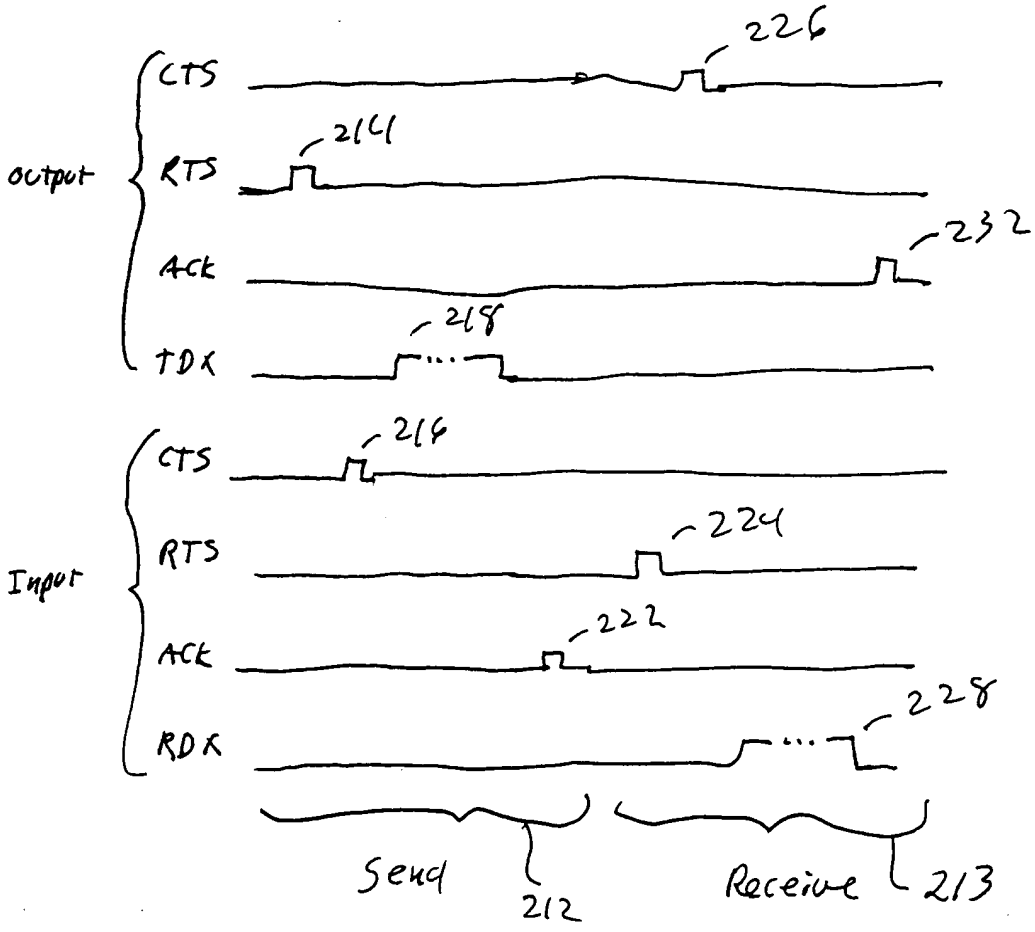


Fig 2 Prior Art

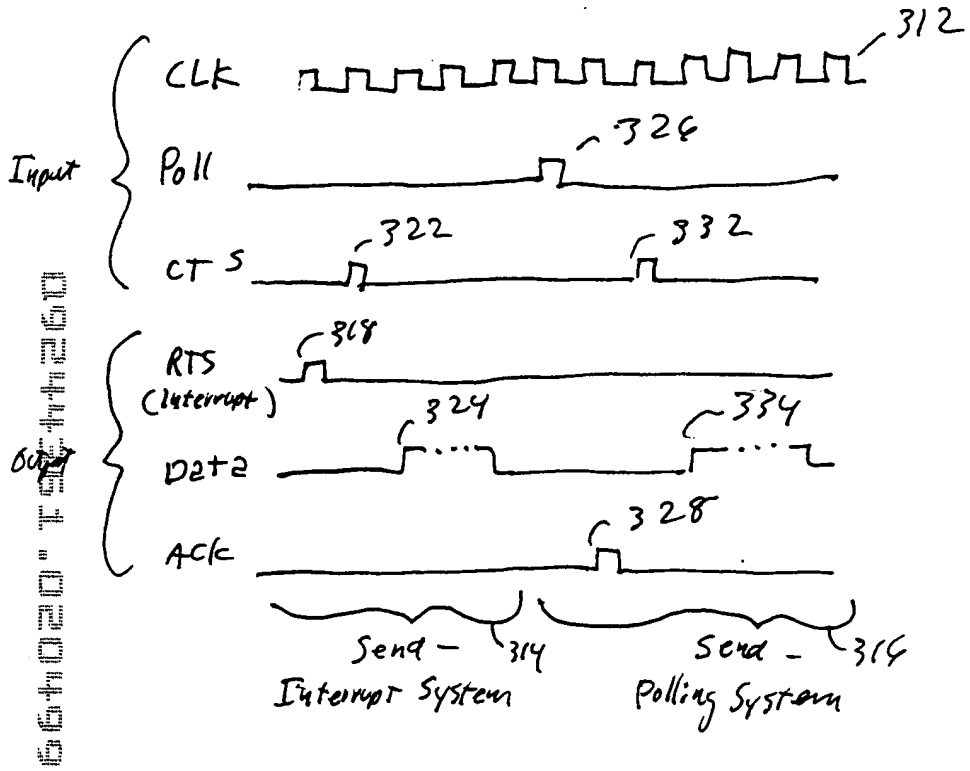


Fig 3 Prior Art

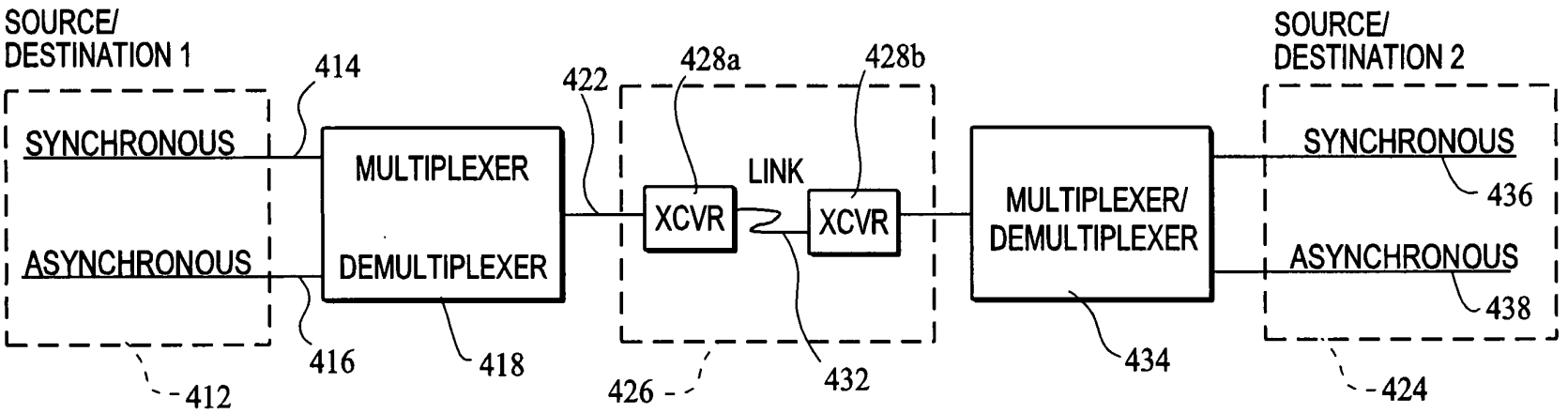


FIG. 4

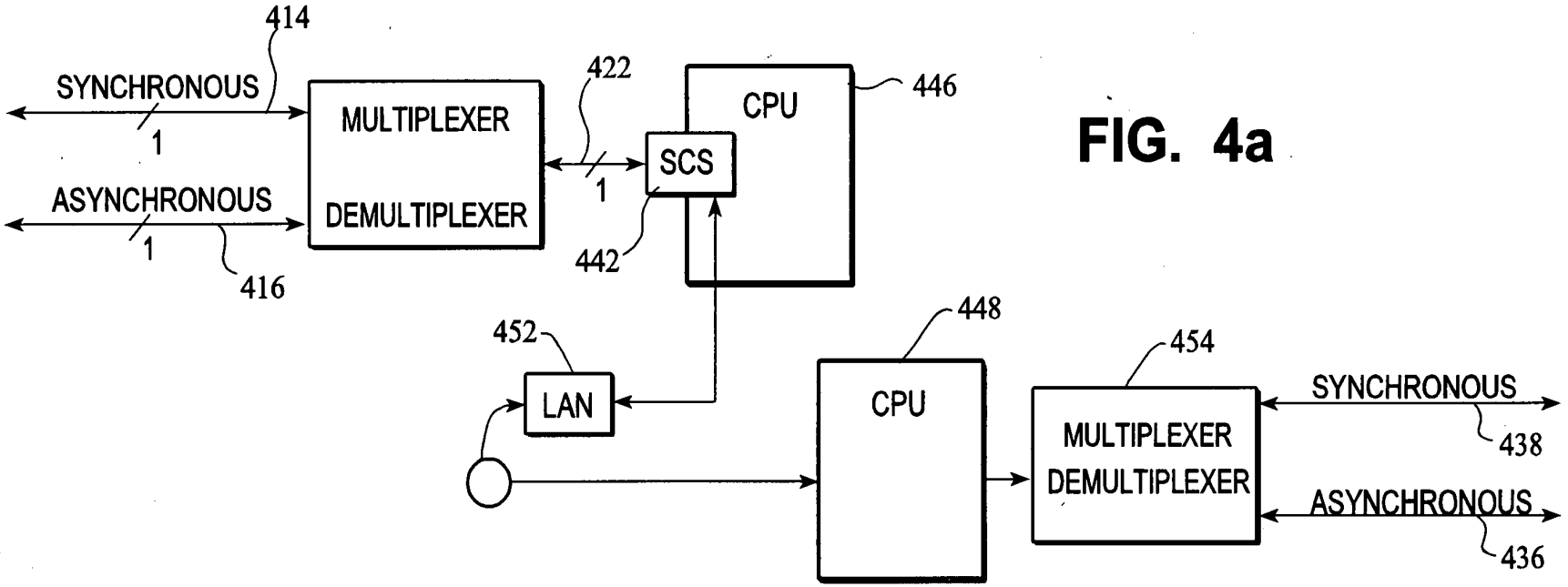


FIG. 4a

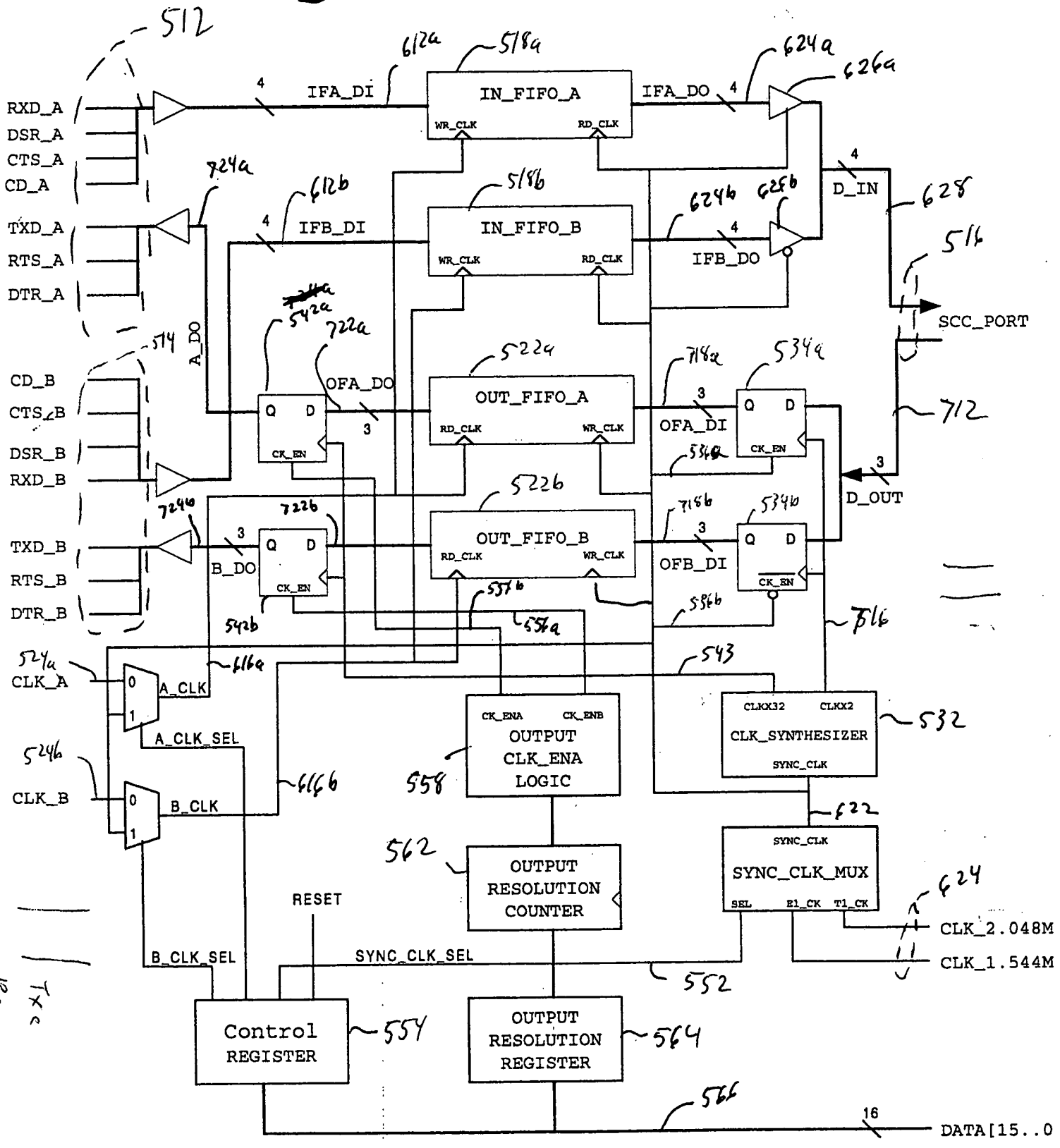


Fig. 5

BLOCK GIAGRAM : TDM OF ASYNCHRONOUS DATA STREAMS

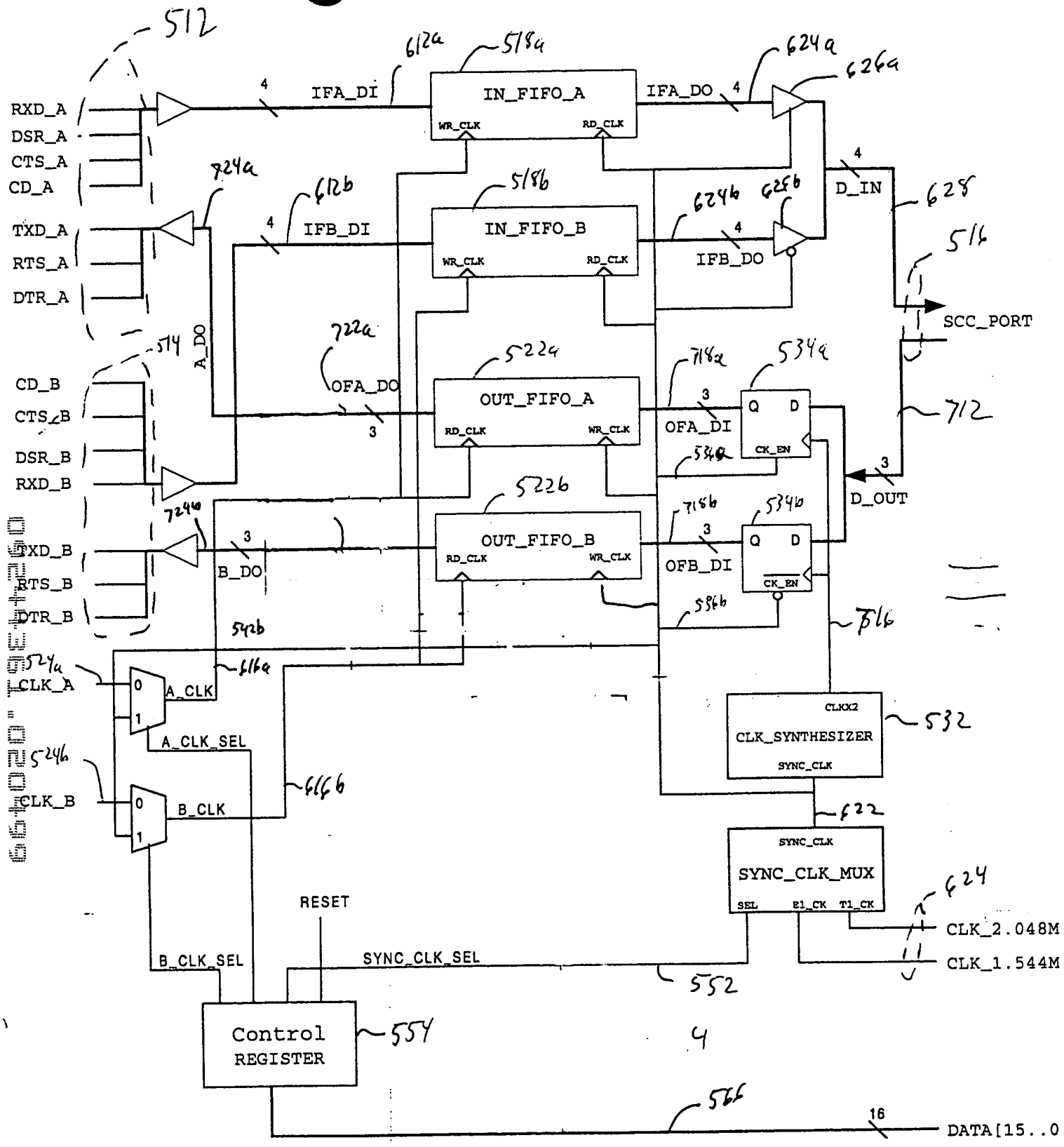
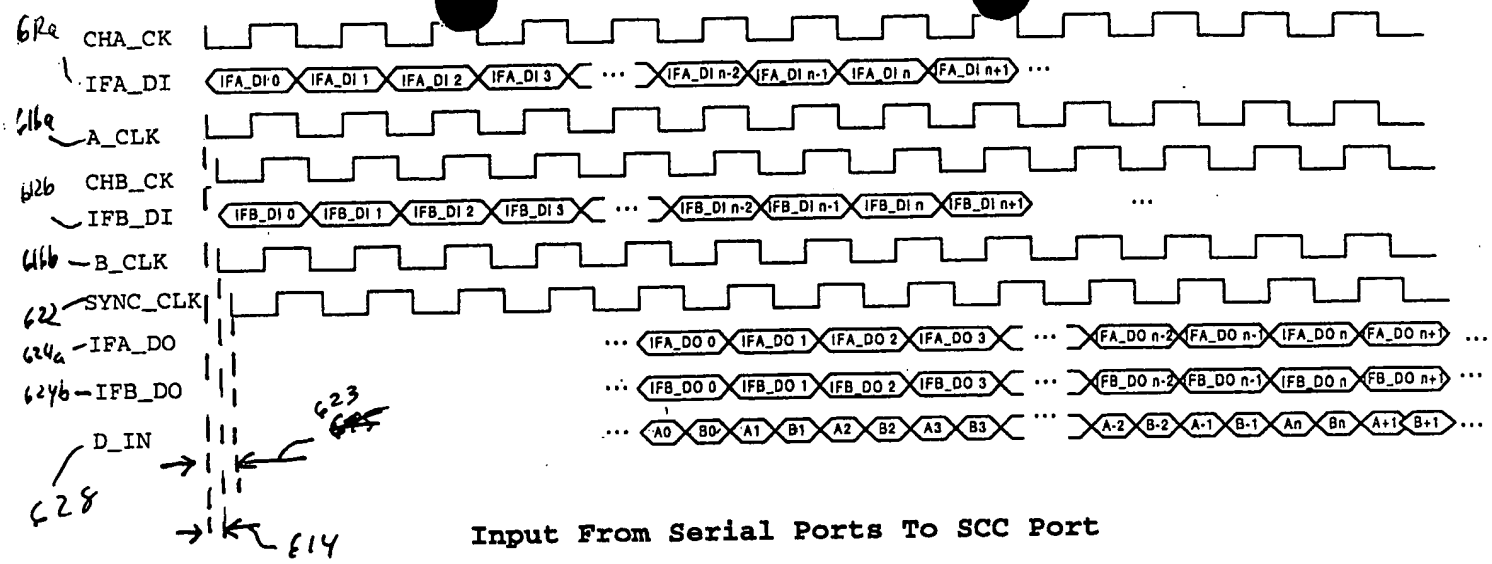


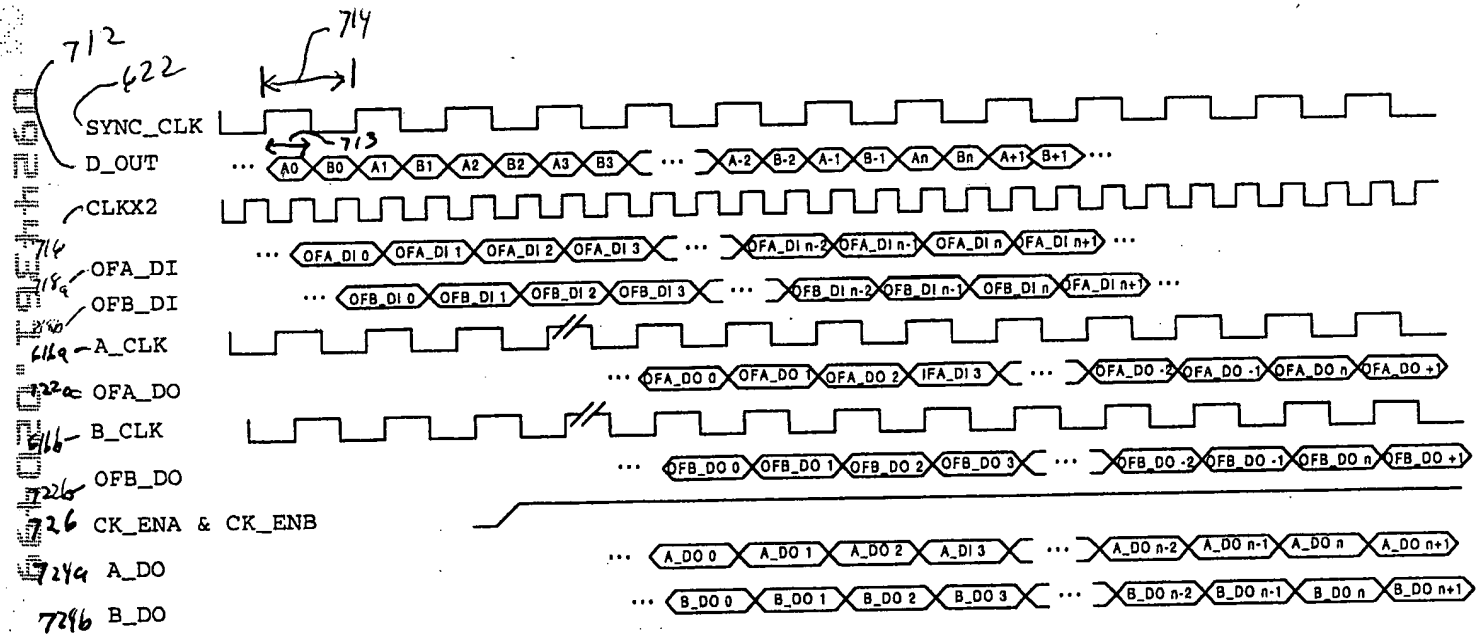
Fig. 5A

BLOCK DIAGRAM : TDM OF ASYNCHRONOUS DATA STREAMS



Input From Serial Ports To SCC Port

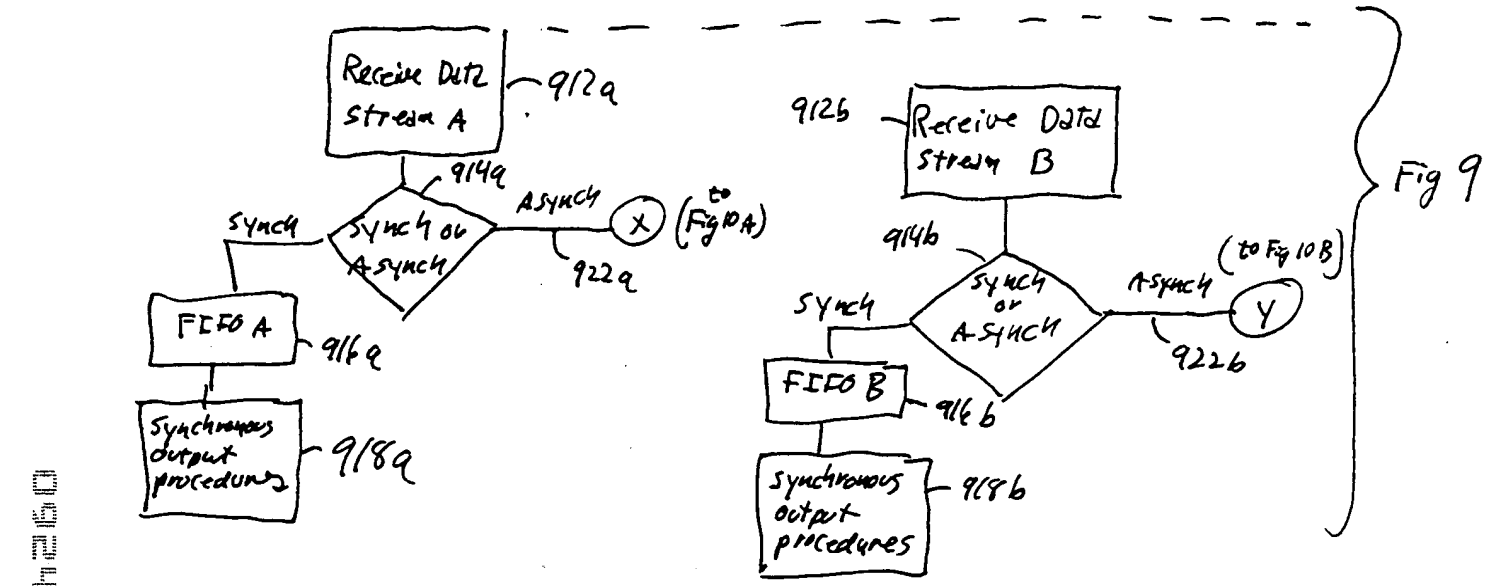
Fig 6

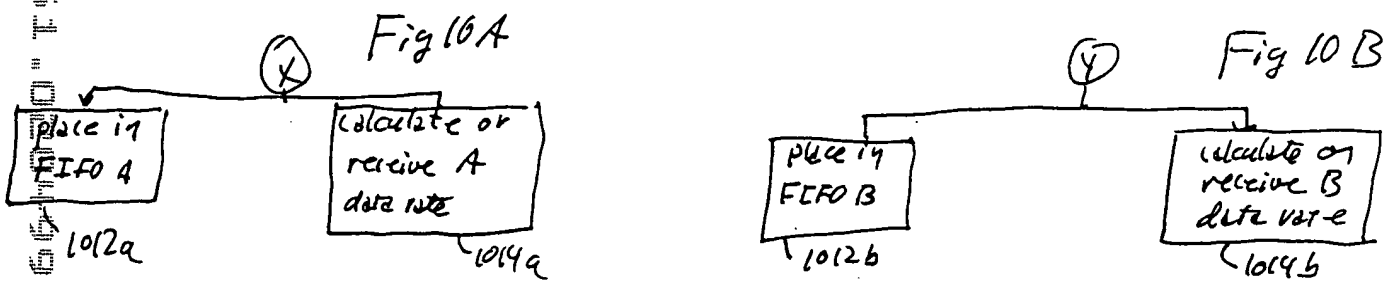


Output From SCC Port To Serial Ports

Fig 7

Case 1 : 2 Synchronous Channels with Same Clock Rate but Clock Skews


Receive Data Stream A
912a
914a
Synch or A-synch
Synch
A-synch
X
(to Fig 10A)
922a
FIFO A
916a
Synchronous output procedures
918a
912b
Receive Data Stream B
914b
Synch or A-synch
(to Fig 10B)
Y
922b
FIFO B
916b
Synchronous output procedures
918b
Fig 9


X
Fig 10A
place in FIFO A
1012a
calculate or receive A data rate
1014a
Y
Fig 10B
place in FIFO B
1012b
calculate or receive B data rate
1014b

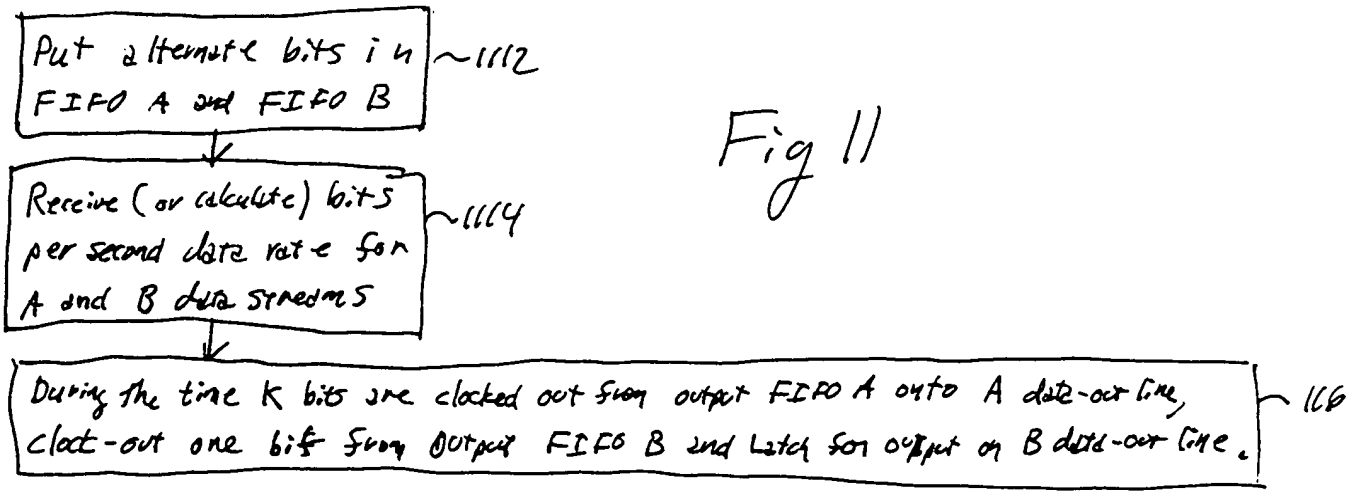

Put alternate bits in FIFO A and FIFO B
1112
Receive (or calculate) bits per second data rate for A and B data streams
1114
During the time K bits are clocked out from output FIFO A onto A data-out line, clock-out one bit from output FIFO B and latch for output on B data-out line.
116

Fig 11

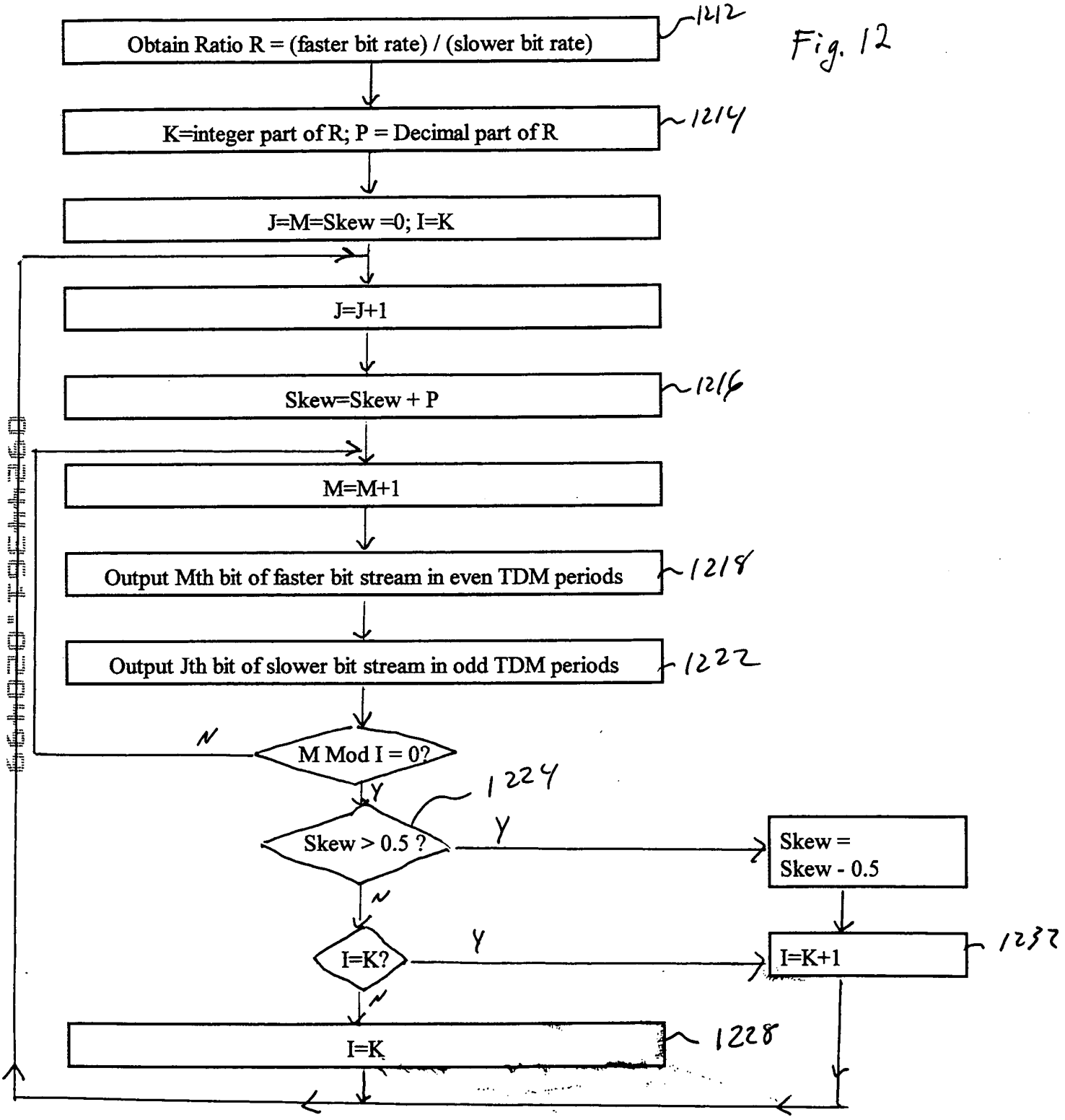


Fig. 12

C:\OFFICE\WPWIN\WPDOCS\CIFIG12.WPD